UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,501	07/10/2003	Takahisa Tanabe	041514-5303	1762

9629 7590 09/21/2004

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,501	TANABE, TAKAHISA	
	Examiner	Art Unit	
	Pho M Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 5* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/10/03 & 12/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 10 July 2003. The information disclosed therein was considered.

Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 04 December 2003. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Jackson et al. (US. 6,683,322).

For the purpose of this rejection, an organic memory layer would be consider as the current voltage apply in memory layer as described in the specification of page 6, lines 20-24.

Regarding claim 1, Jackson et al. in Figure 1 discloses an organic switching memory device comprising:

a plurality of first electrode (first electrode formed by the first conductive layer 320) line;

an organic memory layer (the logic state of memory element is determined by applying a voltage and current to the first electrode, see column 6, lines 2-4) formed on the plurality of first electrode lines (first conductive layer 320) having a voltage current hysteresis characteristic;

a semiconductor diode (diode layer 330) layer stacked (diode layer 330 is formed over the first conductive layer 320 which is including the voltage and current) on the organic memory layer; and

a plurality of second electrode (second electrode formed by the second conductive layer 360) lines formed on the semiconductor diode layer (second electrode 360 is formed over the switch layer 350 that by contact conductor formed over the diode layer 330), the plurality of second electrode (360) lines being disposed in a direction so as to intersect the plurality of first electrode lines (the second conductive layer 360 provides the opposite electrical connection to the memory element of the memory array as the first conductive layer 320).

With respected to claim 2, Jackson et al. disclosed in Figure 3 an organic switching memory device which is the semiconductor diode layer (330) is a pn junction diode layer (see column 4, lines 45-48).

With respected to claim 3, Jackson et al. disclosed in Figure 3 an organic switching memory device which is the semiconductor diode layer is a Schottky diode layer (see column 4, line 45).

Allowable Subject Matter

5. Claims 4-5 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a receiver section for receiving an address designation signal, a data and a write command signal, the address designation signal designating addresses which correspond to intersecting position of the plurality of first electrode line and the plurality of second electrode line" as claimed in the independent claim 4.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hurst et al. (US. 6,646,912) disclosed a memory array comprises first and second sets of transverse electrode separated by a storage layer, which is the memory element, can be switch between the low and high impedance state.

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

pml

PML
15 September 2004

Pho M. Luu
Patent Examiner
Art Unit 2824